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PTO/SB/05 (11-00)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	2204/C01
First Inventor	Erik V. Johnson
Title	See 1 in Addendum
Express Mail Label No.	EL502340748US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [*Total Pages* 18] *(preferred arrangement set forth below)*
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 7]
5. Oath or Declaration [*Total Pages* 3]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 18 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1 33(b).
6. [X] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [X] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Request and Certification under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [ ] Other:

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No _____/_____

Prior application information *Examiner* _____ *Group Art Unit* _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* 28901 *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

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Name (Print/Type)	Jeffrey T. Klayman	*Registration No. (Attorney/Agent)*	39,250
Signature	Jeffrey T. Klayman	*Date*	August 20, 2001

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Addendum

1. Optical Logic Gates Based on Stable, Non-Absorbing Optical Hard Limiters

PTO/SB/17 (12/99)
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See 37 C F.R. §§ 1 27 and 1 28.

TOTAL AMOUNT OF PAYMENT ($) 1,150.00

Complete if Known	
Application Number	
Filing Date	August 20, 2001
First Named Inventor	Erik V. Johnson
Examiner Name	
Group / Art Unit	
Attorney Docket No.	2204/C01

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

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☐ Charge Any Additional Fee Required Under 37 CFR §§ 1 16 and 1 17

2. ☒ **Payment Enclosed:**
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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	710.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	11	-20** = 0	X	18	= 0
Independent Claims	8	- 3** = 5	X	80	= 400
Multiple Dependent					= 0

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 400.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	0.00
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	0.00
139	130	139	130	Non-English specification	0.00
147	2,520	147	2,520	For filing a request for reexamination	0 00
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	0.00
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	0.00
115	110	215	55	Extension for reply within first month	0.00
116	380	216	190	Extension for reply within second month	0.00
117	870	217	435	Extension for reply within third month	0.00
118	1,360	218	680	Extension for reply within fourth month	0.00
128	1,850	228	925	Extension for reply within fifth month	0.00
119	300	219	150	Notice of Appeal	0.00
120	300	220	150	Filing a brief in support of an appeal	0.00
121	260	221	130	Request for oral hearing	0.00
138	1,510	138	1,510	Petition to institute a public use proceeding	0.00
140	110	240	55	Petition to revive - unavoidable	0.00
141	1,210	241	605	Petition to revive - unintentional	0.00
142	1,210	242	605	Utility issue fee (or reissue)	0.00
143	430	243	215	Design issue fee	0.00
144	580	244	290	Plant issue fee	0.00
122	130	122	130	Petitions to the Commissioner	0.00
123	50	123	50	Petitions related to provisional applications	0.00
126	240	126	240	Submission of Information Disclosure Stmt	0.00
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	690	246	345	Filing a submission after final rejection (37 CFR § 1 129(a))	0.00
149	690	249	345	For each additional invention to be examined (37 CFR § 1.129(b))	0.00
Other fee (specify)					0.00
Other fee (specify)					0.00

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 40.00

SUBMITTED BY

Complete *(if applicable)*

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Signature				Date	

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EL502340748US

Practitioner's Docket No. 2204/C01 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Johnson et al.
Application No.: Not yet assigned Group No.:
Filed: 08/20/2001 Examiner:
For: Optical Logic Gates Based on Stable, Non-Absorbing Optical Hard Limiters

Commissioner for Patents
Washington, D.C. 20231

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EL502340748US
Date of Deposit 08/20/2001

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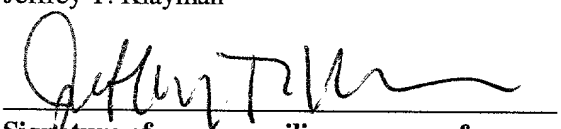
New Utility patent application and documents referenced therein

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. section 1.10, on the date indicated above and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

Jeffrey T. Klayman



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Application Information

Title Line One::	Optical Logic Devices Based on Stable,
Title Line Two::	Non-Absorbing Optical Hard Limiters
Total Drawing Sheets::	7
Formal Drawings?::	Yes
Application Type::	Utility
Docket Number::	14210BAUS02U

Representative Information

Representative Customer Number:: 28901

Continuity Information

This application is a::	Non Prov. of Provisional
> Application One::	60/267,879
Filing Date::	02-09-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR UNITED STATES PATENT

FOR

OPTICAL LOGIC DEVICES BASED ON STABLE, NON-ABSORBING OPTICAL HARD LIMITERS

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Attorney Docket No.: 2204/C01

Client Reference No.: 14210BAUS02U

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OPTICAL LOGIC DEVICES BASED ON STABLE, NON-ABSORBING OPTICAL HARD LIMITERS

PRIORITY

The present application claims priority from United States Provisional Patent Application No. 60/267,879, which was filed on February 9, 2001, and is hereby incorporated herein by reference in its entirety.

CROSS-REFERENCE TO RELATED APPLICATION(S)

The present application may be related to the following commonly owned United States patent application, which is hereby incorporated herein by reference in its entirety:

United States Patent Application No. XX/XXX,XXX entitled **OPTICAL LIMITER BASED ON NONLINEAR REFRACTION**, filed on May 1, 2001 in the names of Edward H. Sargent and Lukasz Brzozowski.

FIELD OF THE INVENTION

The present invention relates generally to optical information processing, and more particularly to optical logic gates based on stable, non-absorbing optical hard limiters.

BACKGROUND OF THE INVENTION

In today's information age, optical communication technologies are being used more and more frequently for transmitting information at very high speeds. Traditionally, information processing equipment (such as switches, routers, and computers) process information electronically. Therefore, optical communications are often converted into electronic form for processing by the information processing equipment. This electronic

processing is slow relative to the speed of the optical communications themselves, and thus often becomes a "bottleneck" of optical communication and processing systems.

SUMMARY OF THE INVENTION

In accordance with one aspect of the invention, various optical logic devices are formed using stable, non-absorbing optical hard limiters. These optical logic devices are able to process information optically without the need to convert the information to an electronic form for processing electronically.

In accordance with another aspect of the invention, an optical gain element is formed using three stable, non-absorbing optical hard limiters.

In accordance with yet another aspect of the invention, an optical AND gate is formed using the transmitted signal of a single stable, non-absorbing optical hard limiter.

In accordance with still another aspect of the invention, an optical OR gate is formed using an optical gain element.

In accordance with still another aspect of the invention, an optical XOR gate is formed by coupling the reflected output of a stable, non-absorbing optical hard limiter as the input to an optical gain element.

In accordance with still another aspect of the invention, an optical NOT gate is formed by coupling the reflected output of a stable, non-absorbing optical hard limiter as the input to an optical gain element.

In accordance with still another aspect of the invention, an optical NAND gate is formed by coupling the output of an optical AND gate as the input to an optical NOT gate.

In accordance with still another aspect of the invention, an optical NOR gate is formed by coupling the output of an optical OR gate as the input to an optical NOT gate.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a schematic block diagram showing the input, transmitted output, and reflected output of an exemplary optical hard limiter in accordance with an embodiment of the present invention;

FIG. 2A is a graph showing the idealized transmitted transfer function of an optical hard limiter in accordance with an embodiment of the present invention;

FIG. 2B is a graph showing the simulated transmitted transfer functions for finite optical hard limiters with different numbers of layers in accordance with an embodiment of the present invention;

FIG. 3 is a graph showing the idealized reflected transfer function of an optical hard limiter in accordance with an embodiment of the present invention;

FIG. 4 is a schematic block diagram showing an optical gain element in accordance with an embodiment of the present invention;

FIG. 5 is a graph showing the idealized transfer function of an optical gain element in accordance with an embodiment of the present invention;

FIG. 6 is a schematic block diagram showing an optical AND gate in accordance with an embodiment of the present invention;

FIG. 7 is a schematic block diagram showing an optical OR gate in accordance with an embodiment of the present invention;

FIG. 8 is a schematic block diagram showing an optical XOR gate in accordance with an embodiment of the present invention;

FIG. 9 is a schematic block diagram showing an optical NOT gate in accordance with an embodiment of the present invention;

FIG. 10 is a schematic block diagram showing an optical NAND gate in accordance with an embodiment of the present invention; and

FIG. 11 is a schematic block diagram showing an optical NOR gate in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

All-optical logic devices are able to process information optically without the need to convert the information to an electronic form for processing electronically.

All-optical logic devices typically either continue to rely on electronic carrier transitions, such as those which rely on semiconductor optical amplifiers, (USP# 5,999,283) or diode/laser/LED/SEED/variable transmission combinations, (USP# 4128300, 4764889), consist of non-integrable systems, (USP# 4932739, 4962987, 4992654, 5078464, 5144375, 5655039, 5831731) narrowly defined devices which can only perform a single operation, (USP# 5315422, 5,831,731), extremely slow devices (US Patents 6005791) or other interference effect devices (USP# 4262992, 5623366). The devices that use carriers do not circumvent the fundamental limit, although they do allow this limit to be more closely approached. These devices are most useful when only the fast components of the nonlinearity are sampled, such as are done in time division demultiplexers. The non-integrable systems, although interesting laboratory experiments and good proofs-of-concept, are not practical for commercial application. The narrowly defined, but integrable, devices do not have the flexibility to enable large scale integration, and since they typically rely on a loss mechanism, such as coupling to a radiative mode, are not efficient for multiple levels of switching.

The all-optical logic devices of the present invention are based on stable non-absorbing optical hard limiters. An exemplary stable, non-absorbing optical hard limiter is described in the related application entitled **OPTICAL LIMITER BASED ON NONLINEAR REFRACTION**, which was incorporated by reference above. Typically, these stable non-absorbing optical hard limiters consist of alternating layers of materials with different linear indices and oppositely signed Kerr coefficients. This construction maintains the center of the stopband in generally the same spectral location, thereby providing stability. The linear and non-linear indices of the layers are such that the material with the lower linear index has a positive Kerr coefficient and the material with the higher linear index has a negative Kerr coefficient. Devices with these properties typically exhibit three regimes of operation, specifically a first regime bounded by input intensities from 0 to I1 in which the signal is completely reflected, a second regime bounded by input intensities from I1 to I2 in which the transmitted signal increases and the reflected signal decreases as intensity increases, and a third regime above input intensity I2 in which all light above a certain level is reflected. The existence of these three regimes enables these devices to be used in optical logic applications. As the nonideality of the device increases, the curve is smoothed. For these devices, I2 is defined as the input intensity at which the built-in optical grating has disappeared completely, and I1 is defined as half of I2. In various embodiments of the present invention, intensity I2 represents a logic one (high), and intensity zero represents a logic zero (low).

FIG. 1 shows a "black box" view of an exemplary optical hard limiter 100. The optical hard limiter 100 outputs a transmitted signal and a reflected signal based upon the intensity of an input signal.

FIG. 2A shows the idealized transmitted transfer characteristics 200 of the optical hard limiter 100. As shown, the transmitted signal is zero for input signals from zero to I1. The transmitted signal increases from zero to I2 as the

input signal increases from I1 to I2. The transmitted signal is limited to I2 for input signals above I2.

In actuality, the transmitted transfer characteristics of the optical hard limiter 100 generally differ from the idealized transmitter transfer characterstics 200 shown in FIG. 2A, and depend upon the number of layers in the optical hard limiter 100. FIG. 2B shows simulated transmitted transfer characteristics 210 for finite devices having different numbers of layers. Devices with more layers approach the piecewise linear behavior of the idealized transmitted transfer characteristics 200 shown in FIG. 2A.

FIG. 3 shows the idealized reflected transfer characteristics 300 of the optical hard limiter 100. As shown, the reflected signal increases from zero to I1 as the input signal increases from zero to I1. The reflected signal decreases from I1 to zero as the input signal increases from I1 to I2. The reflected signal increases as the input signal increases above I2.

As with the transmitted transfer characteristics, the actual reflected transfer characteristics of the optical hard limiter 100 generally differ from the idealized reflected transfer characterstics 300 shown in FIG. 3, and depend upon the number of layers in the optical hard limiter 100. Simulated reflected transfer characteristics for finite devices having different numbers of layers are omitted for convenience.

Various all-optical logic devices make use of the transmitted signal and/or the reflected signal of one or more optical hard limiters. Furthermore, various all-optical logic devices can be combined to form additional all-optical logic devices and circuits. A number of exemplary all-optical logic devices based on stable non-absorbing optical hard limiters are described below. It should be noted that other all-optical logic devices can be formed, and the present invention is not limited to the devices shown or to any particular

devices. It will be apparent to a skilled artisan how other all-optical logic devices can be formed using the described all-optical logic devices.

It should be noted that, in the described all-optical logic devices, signals are often combined in some proportion using a coupler that is external to the optical hard limiter. The described all-optical logic devices are based on a coupler that reduces the signal intensity by half. It should be noted, however, that the present invention is not limited to the use of such couplers or to couplers that reduce the signal intensity by half.

A gain device converts an input signal from {0, I1} to an output signal from {0, I2}. FIG. 4 shows an exemplary all-optical gain device 400 that is created using the transmission characteristics of three optical hard limiters connected in series. The all-optical gain device converts an input signal X1 from {0, I1} to an output signal X2 from {0, I2}. FIG. 5 shows the idealized transfer function 500 of the exemplary gain device 400.

An AND gate outputs a logic one (high) if and only if both inputs are logic one (high) and otherwise outputs a logic zero (low). FIG. 6 shows an exemplary all-optical AND gate 600 that is created using the transmission characteristics of a single optical hard limiter. Inputs X2 and Y2 are combined, and the combined input is fed into an optical hard limiter. The transmitted signal of the optical hard limiter is used as the output of the all-optical AND gate 600. The following table shows the combined input to the limiter and the transmitter signal output of the limiter for the various input signal combinations:

Input X2	Input Y2	Combined input to limiter	Transmitted signal output
0	0	0	0
0	I2	I1	0
I2	0	I1	0
I2	I2	I2	I2

When the input signal X2 is zero (low) and the input signal Y2 is zero (low), the combined input to the limiter is zero (low). The transmitted signal output of the limiter is zero (low) when the input to the limiter is zero (low). Therefore, the output of the all-optical AND gate is zero (low).

When the input signal X2 is zero (low) and the input signal Y2 is one (high), the combined input to the limiter is I1. The transmitted signal output of the limiter is zero (low) when the input to the limiter is I1. Therefore, the output of the all-optical AND gate is zero (low).

When the input signal X2 is one (high) and the input signal Y2 is zero (low), the combined input to the limiter is I1. The transmitted signal output of the limiter is zero (low) when the input to the limiter is I1. Therefore, the output of the all-optical AND gate is zero (low).

When the input signal X2 is one (high) and the input signal Y2 is one (high), the combined input to the limiter is I2. The transmitted signal output of the limiter is one (high) when the input to the limiter is I2. Therefore, the output of the all-optical AND gate is one (high).

An OR gate outputs a logic one (high) if either or both inputs are logic one (high) and otherwise outputs a logic zero (low). FIG. 7 shows an exemplary all-optical OR gate 700 that is created using the all-optical gain device 400. Inputs X2 and Y2 are combined, and the combined input is fed into a gain element 400. The output of the gain element 400 is used as the output of the all-optical OR gate 700. The following table shows the combined input to the gain element 400 and the gain element output for the various input signal combinations:

Input X2	Input Y2	Combined input to gain element	Gain element output

0	0	0	0
0	I2	I1	I2
I2	0	I1	I2
I2	I2	I2	I2

When the input signal X2 is zero (low) and the input signal Y2 is zero (low), the combined input to the gain element is zero (low). The gain element outputs a zero (low) when its input is zero (low). Therefore, the output of the all-optical OR gate is zero (low).

When the input signal X2 is zero (low) and the input signal Y2 is one (high), the combined input to the gain element is I1. The gain element outputs a one (high) when its input is I1. Therefore, the output of the all-optical OR gate is one (high).

When the input signal X2 is one (high) and the input signal Y2 is zero (low), the combined input to the gain element is I1. The gain element outputs a one (high) when its input is I1. Therefore, the output of the all-optical OR gate is one (high).

When the input signal X2 is one (high) and the input signal Y2 is one (high), the combined input to the gain element is I2. The gain element outputs a one (high) when its input is I2. Therefore, the output of the all-optical OR gate is one (high).

An XOR (exclusive-OR) gate outputs a logic one (high) if either one but not both inputs are a logic one (high) and otherwise outputs a logic zero (low). FIG. 8 shows an exemplary all-optical XOR gate 800 that is created using the reflected signal of an optical hard limited in series with an all-optical gain device 400. Inputs X2 and Y2 are combined, and the combined input is fed into an optical hard limiter. The reflected signal of the optical hard limiter is fed into a gain element 400. The output of the gain element 400

is used as the output of the all-optical XOR gate 800. The following table shows the combined input to the limiter, the reflected signal output to the gain element 400, and the gain element output for the various input signal combinations:

Input X2	Input Y2	Combined input to limiter	Reflected signal output to gain element	Gain element output
0	0	0	0	0
0	I2	I1	I1	I2
I2	0	I1	I1	I2
I2	I2	I2	0	0

When the input signal X2 is zero (low) and the input signal Y2 is zero (low), the combined input to the limiter is zero (low). The reflected signal output of the limiter is zero (low) when the input to the limiter is zero (low). The gain element outputs a zero (low) when its input is zero (low). Therefore, the output of the all-optical XOR gate is zero (low).

When the input signal X2 is zero (low) and the input signal Y2 is one (high), the combined input to the limiter is I1. The reflected signal output of the limiter is I1 when the input to the limiter is I1. The gain element outputs a one (high) when its input is I1. Therefore, the output of the all-optical XOR gate is one (high).

When the input signal X2 is one (high) and the input signal Y2 is zero (low), the combined input to the limiter is I1. The reflected signal output of the limiter is I1 when the input to the limiter is I1. The gain element outputs a one (high) when its input is I1. Therefore, the output of the all-optical XOR gate is zero (low).

When the input signal X2 is one (high) and the input signal Y2 is one (high), the combined input to the limiter is I2. The reflected signal output of

the limiter is zero (low) when the input to the limiter is I2. The gain element outputs a zero (low) when its input is zero (low). Therefore, the output of the all-optical AND gate is one (high).

A NOT gate outputs a logic one (high) if a single input is a logic zero (low) and outputs a logic zero (low) if the single input is a logic one (high). FIG. 9 shows an exemplary all-optical NOT gate 900 that is created using the reflected signal of an optical hard limited in series with an all-optical gain device 400. The all-optical NOT gate 900 is a special case of the all-optical XOR gate 800 in which the input Y2 is fixed at a logic one (high). Without further explanation, the following table shows the combined input to the limiter, the reflected signal output to the gain element 400, and the gain element output for the various input signal combinations:

Input X2	Fixed input I2	Combined input to limiter	Reflected signal output to gain element	Gain element output
0	I2	I1	I1	I2
I2	I2	I2	0	0

Additional all-optical logic gates and circuits can be formed using the transmitted and reflected signals of the optical hard limiter. Furthermore, the all-optical logic gates described above can be used as building blocks to form additional all-optical logic gates and circuits.

FIG. 10 shows an all-optical NAND gate 1000 formed by coupling the output of an all-optical AND gate 600 as the input to an all-optical NOT gate 900.

FIG. 11 shows an all-optical NOR gate 1100 formed by coupling the output of an all-optical OR gate 700 as the input to an all-optical NOT gate 900.

Additional considerations are discussed in E.V. Johnson, **ALL-OPTICAL SIGNAL PROCESSING AND PACKET FORWARDING USING NONMONOTONIC INTENSITY TRANSFER CHARACTERISTICS**, a thesis submitted in conformity with the requirements for the degree of Master of Applied Science, Graduate Department of Electrical and Computer Engineering, University of Toronto (2001), which is hereby incorporated herein by reference in its entirety.

The present invention may be embodied in other specific forms without departing from the true scope of the invention. The described embodiments are to be considered in all respects only as illustrative and not restrictive.

What is claimed is:

1. An optical logic device for processing information optically using the transmitted and/or reflected characteristics of at least one stable, non-absorbing optical hard limiter.

2. The optical logic device of claim 1, wherein the at least one stable, non-absorbing optical hard limiter comprises alternating layers of materials with different linear indices and oppositely signed Kerr coefficients.

3. The optical logic device of claim 1, wherein the transmitted characteristics of a stable, non-absorbing optical hard limiter comprise:

a first range bounded by input signals in the range of approximately zero to I1 in which the transmitted output signal of the stable, non-absorbing optical hard limiter is approximately zero;

a second range bounded by input signals in the range approximately from I1 to I2 in which the transmitted output signal of the stable, non-absorbing optical hard limiter increases from zero to I2; and

a third range bounded by input signals in the range above approximately I2 in which the transmitted output signal of the stable, non-absorbing optical hard limiter is approximately I2, where I1 is approximately half of I2.

4. The optical logic device of claim 1, wherein the reflected characteristics of a stable, non-absorbing optical hard limiter comprise:

a first range bounded by input signals in the range of approximately zero to I1 in which the reflected output signal of the stable, non-absorbing optical hard limiter approximately equal to the input signal;

a second range bounded by input signals in the range approximately from I1 to I2 in which the reflected output signal of the stable, non-absorbing optical hard limiter decreases from approximately I1 for an input signal of I1 to approximately zero for an input signal of I2; and

a third range bounded by input signals in the range above approximately I2 in which the reflected output signal of the stable, non-absorbing optical hard limiter is increases as the input signal increases above I2, where I1 is approximately half of I2.

5. An optical gain element for converting an optical input signal having an intensity substantially from the set {0, I1} to an optical output signal having an intensity substantially from the set {0, I2}, where I1 is approximately half of I2, the all-optical gain element comprising:

a first stable, non-absorbing optical hard limiter operably coupled to receive as its input a combination of the optical input signal and a signal having an intensity of approximately 4 I1 combined in an approximately 80:20 ratio;

a second stable, non-absorbing optical hard limiter operably coupled to receive as its input a combination of the transmitted output signal from the first stable, non-absorbing optical hard limited and a signal having an intensity of approximately 5 I1 combined in an approximately 80:20 ratio; and

a third stable, non-absorbing optical hard limiter operably coupled to receive as its input a combination of the transmitted output signal from the second stable, non-absorbing optical hard limited and a signal having an intensity of approximately 4.88 I1 combined in an approximately 80:20 ratio and to output its transmitted signal as the output of the optical gain element.

6. An optical AND gate comprising a stable, non-absorbing optical hard limiter operably coupled to receive as its input a combination of a first input signal and a second input signal combined in an approximately 50:50 ratio and to output its transmitted signal as the output of the optical AND gate, wherein:

the combined input signal is approximately zero and the output of the optical AND gate is approximately zero when both the first input signal and the second input signal are zero;

the combined input signal is approximately I1 and the output of the optical AND gate is approximately zero when the first input signal is zero and the second input signal is I2;

the combined input signal is approximately I1 and the output of the optical AND gate is approximately zero when the first input signal is I2 and the second input signal is zero;

the combined input signal is approximately I2 and the output of the optical AND gate is approximately I2 when the first input signal is I2 and the second input signal is I2; and

I1 is approximately half of I2.

7. An optical OR gate comprising an optical gain element for converting an optical input signal having an intensity substantially from the set {0, I1} to an optical output signal having an intensity substantially from the set {0, I2, wherein the optical gain element is operably coupled to receive as its input a combination of a first input signal and a second input signal combined in an approximately 50:50 ratio and to output the converted signal as the output of the optical OR gate, and wherein:

the combined input signal is approximately zero and the output of the optical OR gate is approximately zero when both the first input signal and the second input signal are zero;

the combined input signal is approximately I1 and the output of the optical OR gate is approximately I2 when the first input signal is zero and the second input signal is I2;

the combined input signal is approximately I1 and the output of the optical OR gate is approximately I2 when the first input signal is I2 and the second input signal is zero;

the combined input signal is approximately I2 and the output of the optical OR gate is approximately I2 when the first input signal is I2 and the second input signal is I2; and

I1 is approximately half of I2.

8. An optical XOR gate comprising:

a stable, non-absorbing optical hard limiter operably coupled to receive as its input a combination of a first input signal and a second input signal combined in an approximately 50:50 ratio; and

an optical gain element for converting an optical input signal having an intensity substantially from the set {0, I1} to an optical output signal having an intensity substantially from the set {0, I2}, the optical gain element operably coupled to receive as its input a reflected signal from the stable, non-absorbing optical hard limiter and to output the converted signal as the output of the optical XOR gate, wherein:

the combined input signal is approximately zero, the reflected signal is approximately zero, and the output of the optical XOR gate is approximately zero when both the first input signal and the second input signal are zero;

the combined input signal is approximately I1, the reflected signal is approximately I1, and the output of the optical XOR gate is approximately I2 when the first input signal is zero and the second input signal is I2;

the combined input signal is approximately I1, the reflected signal is approximately I1, and the output of the optical XOR gate is approximately I2 when the first input signal is I2 and the second input signal is zero;

the combined input signal is approximately I2, the reflected signal is approximately zero, and the output of the optical XOR gate is approximately zero when the first input signal is I2 and the second input signal is I2; and

I1 is approximately half of I2.

9. An optical NOT gate comprising:

a stable, non-absorbing optical hard limiter operably coupled to receive as its input a combination of an input signal and a fixed signal of approximate intensity I2 combined in an approximately 50:50 ratio; and

an optical gain element for converting an optical input signal having an intensity substantially from the set {0, I1} to an optical output signal having an intensity substantially from the set {0, I2}, the optical gain element operably coupled to receive as its input a reflected signal from the stable, non-

absorbing optical hard limiter and to output the converted signal as the output of the optical NOT gate, wherein:

the combined input signal is approximately I1, the reflected signal is approximately I1, and the output of the optical NOT gate is approximately I2 when the input signal is zero;

the combined input signal is approximately I2, the reflected signal is approximately zero, and the output of the optical NOT gate is approximately zero when the input signal is I2; and

I1 is approximately half of I2.

10. An optical NAND gate comprising:

an optical AND gate; and

an optical NOT gate operably coupled to an output of the optical AND gate for logically inverting the output of the optical AND gate, wherein the optical AND gate and the optical NOT gate are based on stable, non-absorbing optical hard limiters.

11. An optical NOR gate comprising:

an optical OR gate; and

an optical NOT gate operably coupled to an output of the optical OR gate for logically inverting the output of the optical OR gate, wherein the optical OR gate and the optical NOT gate are based on stable, non-absorbing optical hard limiters.

ABSTRACT OF THE DISCLOSURE

Various optical logic devices are formed using stable, non-absorbing optical hard limiters. These optical logic devices are able to process information optically without the need to convert the information to an electronic form for processing electronically.

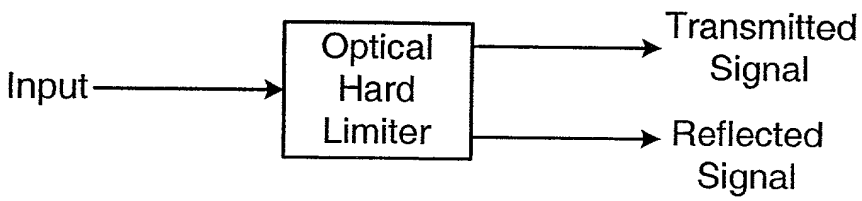
Input
Optical
Hard
Limiter
Transmitted
Signal
Reflected
Signal

FIG. 1 100

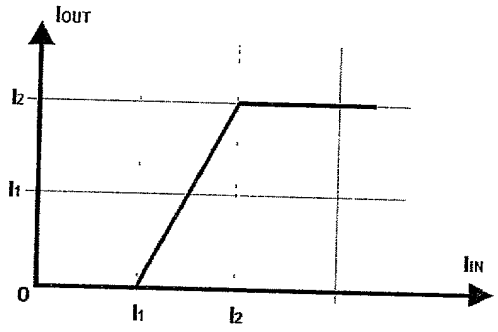

FIG. 2A 200

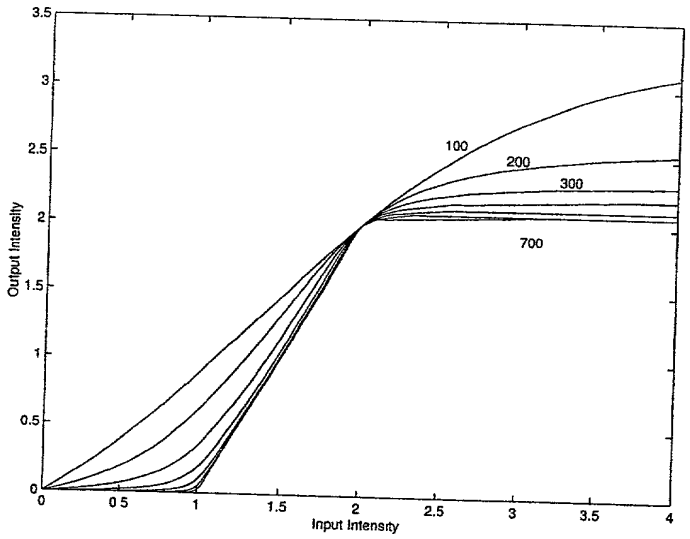

FIG. 2B 210

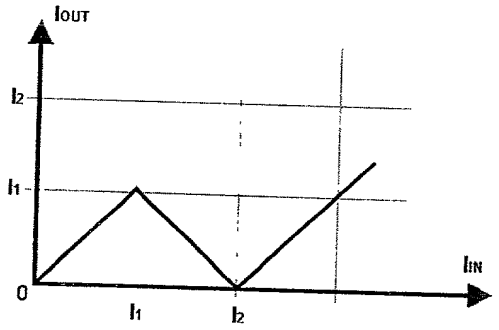

FIG. 3 300

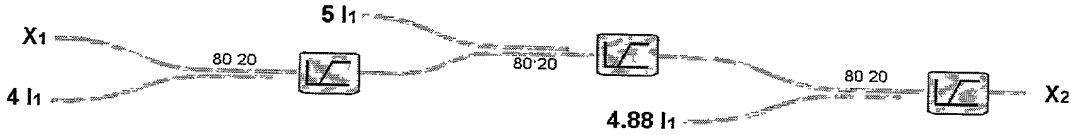

FIG. 4 400

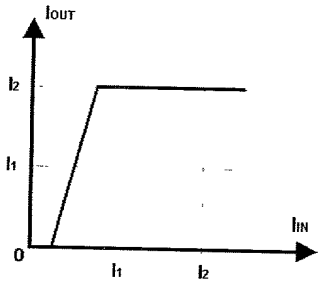

FIG. 5 500

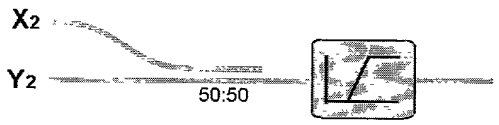

FIG. 6 600

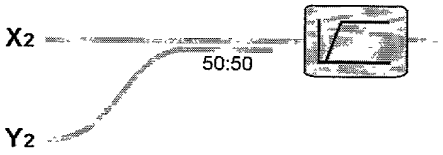

FIG. 7 700

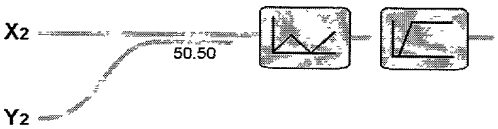

FIG. 8 800

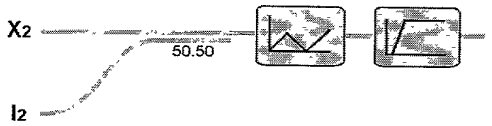

FIG. 9 900

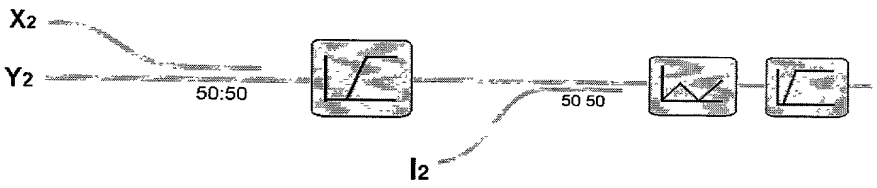

FIG. 10 1000

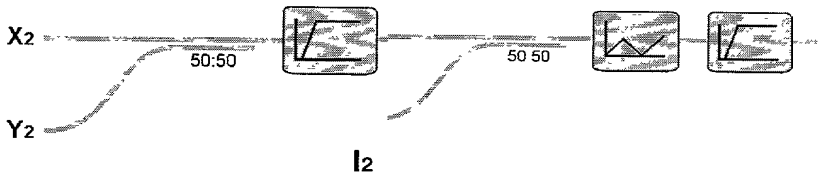

FIG. 11 1100

Docket No.
2204/C01

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Optical Logic Gates Based on Stable, Non-Absorbing Optical Hard Limiters

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

60/267,879	February 9, 2001
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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Sole or first inventor's signature

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